REMARKS

Claims 1-19 are pending. Claims 1-3 are amended and new claim 19 is added.

Claims 1, 3, 4 and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Minami (U.S.P. 4,252,840) in view of Dennison et al. (U.S.P. 5,338,700). Favorable reconsideration is earnestly solicited.

Semiconductor devices often require very thick inter-layer insulation film. In the methods for fabricating such the semiconductor devices, deep through-holes penetrating through the thick inter-layer insulation film must be formed. It is important that the deep through-holes are formed while suppressing the etching damage to the base structures, such as the semiconductor substrate, transistors, etc. Generally, over-etching of about 5O-1OO% of film thickness is performed so as to completely open the through-hole even if the film thickness of the insulation film is fluctuated in the film forming step. The over-etching amount is increased the thickness of the insulation film is increased, and the etching damage to the base structures is also increased. Thus, the technology for reducing the etching damage to the base structures with satisfying the request for making the insulation film thicker is expected.

Then, in the present invention, in order to easily form the hole penetrating through the thick insulation film, the first insulation film, the second insulation film and the third insulation film which have different etching characteristics from each other are formed, and the first insulation film has a substantially flat surface.

When the insulation film is formed of three insulation films which have different etching characteristics from each other and the insulation films are etched one by one to form the hole, over-etching amounts of the insulation films can be set according to each thickness. Thus, the over-etching amount for etching the lowermost insulation film (the first insulation film) can be much decreased in comparison with the over-etching amount for etching a single insulation film having the same thickness as the total thickness of the three insulation films. Additionally, the etching selective ratio required for the base structures (e.g., the etching stopper film for the self aligned contact) can be lowered.

The reason why the first insulation film having a substantially flat surface is formed is for increasing the etching selective ratio with respect to the second insulation film when the third insulation film is etched to form the hole. When the first insulation film has a substantially flat surface, the second insulation film formed over the first insulation film can have also a substantially flat surface. The insulation film formed over the flat surface can have a high etching selective ratio by comparison with the etching selective ratio of the insulation film formed over the slant portion (see, e.g., the fourth embodiment of the present application). Thus, the third insulation film can be etched with a high etching selective ratio by using the second insulation film as a stopper, and the second insulation film can be much thinner than the third insulation film, The over-etching amount for etching the second insulation film can be also decreased.

Thus, according to the present invention, the hole can be easily formed in the thick insulation film while suppressing the etching damage to the base structures.

Minami discloses a method for fabricating a semiconductor device including the steps of: forming a gate electrode 4 on the semiconductor substrate; forming a first insulation film 7 covering the gate electrode 4; forming a second insulation film 10 on the first insulation film 7; forming a third insulation film 11 on the second insulation film 10; forming over the third insulation film 11 a mask layer; and forming a contact hole 12 in the third insulation film 11, the second insulation film 10 and the first insulation film 7.

However, in Minami, the first insulation film 7 does not have a substantially flat surface. The second insulation film 10 is not thinner than the third insulation film 11. Although the third insulation film 11 and the second insulation film 10 are etched in the step of forming the contact hole 12, the first insulation film 7 is not etched (see, e.g., FIG. 1F).

In Minami, when the second insulation film 10 is thinner than the third insulation film 11, in other words, when the third insulation film 11 is thicker than the second insulation film 10, it becomes difficult to form the interconnection 15 in the contact hole 12 and the prescribed wiring region 13, because the bottom of the contact hole 12 and the bottom of the prescribed wiring region 13 are located in a very deep portion of the insulating films 7, 10, 11. Thus, according to the disclosure of Minami, one of ordinary skill in the art would not set the thickness of the second insulation film 10 to be thinner than the thickness of the third insulation film 11.

In Minami, the first insulation film 7 in a region for the contact hole 12 is removed before the formation of the second insulation film 10 and the third insulation film 11 in advance in order to simultaneously form the contact hole 12 and the prescribed wiring region 13 in the second and

the third insulation films 10, 11. Thus, according to the disclosure of Minami, one of ordinary skill in the art would not sequentially etch the first to the third insulation films 7, 10, 11 to form the contact hole 12.

Minami neither teaches nor suggests that the surface of the first insulation film 7 is planarized, the thickness of the second insulation film 10 is set to be thinner than that of the third insulation film, and the first to the third insulation films 7, 10, 11 are sequentially etched to form the contact hole 12.

Thus, Minami is clearly different from the present invention and does not provide any motivation for the present invention.

Dennison et at discloses that the insulation film is planarized by chemical mechanical polishing. However, as described above, Minami is clearly different from the present invention and does not provide any motivation for the present invention.

Thus, the present invention would not have been obvious to one of ordinary skill in the art at the time the invention was made, even if both of Minami and Dennison et at are considered.

Claims 6-8, 9-11 and 12-14 were rejected under 35 U.S.C. §102(e) as being anticipated by Ema et al. (U.S.P. 6,744,091) and Claims 6, 17 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ema et al.

Ema et al. is a divisional application (No. 09/637,256) of the parent application (No. 09/037,068, now U.S.P, 6,395,599) of the present application. That is, Ema et at and the present

application are based on the same application. Thus, the present application can not be rejected based on Ema et al.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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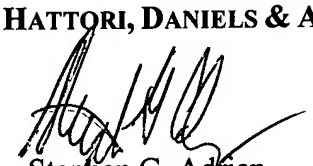

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Attachment: Request for Continued Examination